GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS AND COMMUNICATION ENGINEERING (11)
VLSI TECHNOLOGY & DESIGN
SUBJECT CODE: 2161101
B.E. 6th SEMESTER

Type of course: MOSFET Device and Circuit course

Prerequisite: Knowledge of Basic and Digital Electronics

Rationale: This course will provide an opportunity to the students to learn about various topics VLSI such as MOSFET fabrication, its physics, and analysis as well as design of digital circuits using MOSFET device. In laboratory part of this course, students will be given exposure to hardware description language such as VHDL/verilog for automated design of digital circuits. This subject is very important for the students who will be in future would like to pursue their career in VLSI domain.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
				Theory Marks			Practical Marks			
L	T	P	C	ESE (E)	PA (M)		ESE (V)		PA (I)	
					PA	ALA	ESE	OEP		
4	0	2	6	70	20	10	20	10	20	100

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Introduction:** Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, introduction to FPGA and CPLD, computer aided design technology.	4	8
2	**Fabrication of MOSFET :** Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.	4	8
3	**MOS Transistor:** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances	8	16
4	**MOS Inverters: Static Characteristics:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement and Depletion type MOSFET load), CMOS Inverter	7	13
5	**MOS Inverters Switching characteristics and Interconnect Effects :** Introduction, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters	8	16

6	**Combinational MOS Logic Circuits:** Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs)	**5**	**9**
7	**Sequential MOS Logic Circuits :** Introduction, Behavior of Bistable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop	**4**	**8**
8	**Dynamic Logic Circuits :** Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-performance Dynamic CMOS circuits	**7**	**12**
9	**Chip I/P and O/P Circuits :** On chip Clock Generation and Distribution, Latch –Up and its Prevention	**2**	**4**
10	**Design for testability :** Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques, built-in Self Test (BIST) techniques, current monitoring IDDQ test	**3**	**6**

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
10	**15**	**10**	**20**	**10**	**5**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici, TATA McGraw-Hill Pub. Company Ltd.
2. Basic VLSI Design By Pucknell and Eshraghian, PHI,3rd ed.
3. Introduction to VLSI Systems by Mead C and Conway, Addison Wesley
4. Introduction to VLSI Circuits & Systems – John P. Uyemura
5. Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic

Course Outcome:

After learning the course the students should be able to:

1. Explain fabrication of MOSFET based circuits
2. Describe working of MOSFET and its mathematical model
3. Prepare layout of MOSFET based circuits
4. Analyze, design, and simulate various MOSFET based inverter circuits
5. Realize and size given logic function using MOSFETs
6. Analyze, design, and simulate Dynamic CMOS circuits
7. Explain importance of interconnect parasitic

8. Explain importance of CMOS latch-up, clocking strategy, and testing principles
9. Explain architecture of FPGA and CPLD
10. Write programs in VHDL for digital circuits and realize them on FPGA/CPLD

List of Experiments:

1. Minimum 9 practicals Based on VHDL/Verilog
2. Minimum 3 Practicals Based on Pspice/spice of MOSFET Characteristics
3. Minimum 2 Practicals on Layout Tools

VLSI design methodologies should be covered during Laboratory sessions.
Suggested List of Experiments

1. Introduction to programmable devices (FPGA, CPLD), Hardware Description Language (VHDL), and the use programming tool.
1. Implementation of basic logic gates and its testing.
2. Implementation of adder circuits and its testing.
3. Implementation 4 to 1 multiplexer and its testing.
4. Implementation of 3 to 8 decoder and its testing.
5. Implementation of 8 to 3 priority encoder and its testing.
6. Implementation of J-K and D Flip Flops and its testing.
7. Implementation of sequential adder and its testing.
8. Implementation of BCD counter and its testing.
9. Implementation of two 8-bit multiplier circuit and its testing.
10. Simulation of CMOS Inverter using SPICE for transfer characteristic.
11. Simulation and verification of two input CMOS NOR gate using SPICE.
12. Implementation and simulation of given logic function using dynamic logic.
13. To generate layout for CMOS Inverter circuit and simulate it for verification.
14. To prepare layout for given logic function and verify it with simulations.
15. To measure $I_{DS} – V_{GS}$ and $I_{DS} – V_{DS}$ characteristics of given n-channel and p-channel MOSFETs.
16. To measure propagation delay of a given CMOS Inverter circuit.

Design based Problems (DP)/Open Ended Problem:

1. Design and verify CMOS Inverter circuit.
2. Write and verify VHDL/Verilog program for practical applications of your choice (e. g. lift controller).
3. Design and verify dynamic CMOS circuit.
4. Design and verify MOSFET based voltage bootstrapping circuit.

Major Equipment/software:

Circuit simulator, FPGA/CPLD programming tool, Multimeter, Power supply, function generator, oscilloscope

List of Open Source Software/learning website: NPTEL, NGspice circuit simulator

ACTIVE LEARNING ASSIGNMENTS: Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to GTU.